Amendment to the preface to the claims

Please amend the preface prior to the claims from "Claims" to "I Claim".

Amendment to Claims

Please amend the claims as shown below.

Claims 1 – 20 (Previously Cancelled Without Traverse)

21. (Currently Amended) A high-speed transmitter for digital data having a variable data rate, the transmitter comprising:

a convolutional encoder, adapted to generate, for each group of k input bits in ~~the~~ a bitstream, n coded output bits, such that k and n are integers, n equal to or greater than k, and at least one of k and n is variable responsive to the variable data rate of the transmitter; ~~and~~

a modulator, coupled to map the output bits generated by the encoder to a constellation of M symbols for transmission by the transmitter, M an integer, which is variable responsive to the variable data rate of the transmitter[.]; and

wherein for a given rate RS of transmission of the symbols by the transmitter, the variable data rate Rb is given by Rb = Rs * log2(M) * Rc, wherein Rc is a code rate equal to k/n.

22. Cancel claim 22.

23. (Currently Amended) A transmitter according to claim ~~2221~~, wherein the rate of transmission of the symbols is substantially fixed at a standard rate.

24. (Original) A transmitter according to claim 23, wherein the standard rate is substantially equal to 11 million symbols per second.

25. (Original) A transmitter according to claim 21, wherein the constellation comprises a phase-shift-keyed constellation of order M.

26. (Original) A transmitter according to claim 25, wherein after mapping the output bits to the symbols, the modulator is adapted to rotate a phase of the symbols in accordance with a pseudo-random cover function.

27. (Original) A transmitter according to claim 21, wherein the encoder comprises a sequence of delay stages coupled to receive the input bits in a serial stream, and a plurality of adders, which are coupled to receive the input bits from the delay stages and to add the input bits together so as to generate at least two of the coded output bits in parallel.

28. (Original) A transmitter according to claim 27, wherein the modulator is configured to select the coded output bits from the encoder to be mapped to each of the symbols responsive to the variable data rate.

29. (Currently Amended) A method for variable-rate, high-speed transmission of digital data, comprising:

specifying a first bit rate at which the data are to be transmitted by a transmitter;

applying convolutional encoding to the data so as to generate, for each group of k input bits in ~~the~~ a bitstream, n coded output bits, such that k and n are integers, n equal to or greater than k;

modulating the output bits to generate a constellation of M symbols, M a variable integer, for transmission of the modulated data at a given symbol rate and at the first bit rate;

specifying a second bit rate at which the data are to be transmitted, different from the first bit rate; ~~and~~

changing a value of at least one of k, n and M, so that after applying the convolutional encoding and modulating the output bits using the changed value, the transmitter transmits the modulated data at the given symbol rate and at the second bit rate[.]; and

wherein for the given symbol rate R5, changing the value of at least one of k, n and M comprises changing the value so that the second bit rate Rb is given by Rb = RS * log2(M) * Rc, wherein R, is a code rate equal to k/n.

30. Cancel claim 30.

31. (Currently Amended) A method according to claim ~~30~~29, wherein the symbol rate is substantially equal to 11 million symbols per second.

32. (Original) A method according to claim 29, wherein modulating the output bits comprises applying phase shift keying of order M to generate the symbols.

33. (Original) A method according to claim 32, and comprising rotating a phase of the symbols in accordance with a pseudo-random cover function.

34. (Original) A method according to claim 29, wherein applying the convolutional encoding comprises passing the input bits in a serial stream through a sequence of delay stages, and adding the input bits from the delay stages together so as to generate at least two of the coded output bits in parallel.

35. (Original) A method according to claim 34, wherein modulating the output bits comprises selecting the coded output bits to be mapped to each of the symbols responsive to the variable data rate.